REMARKS

Reconsideration of the application is respectfully requested.

Claims 1-4 are pending and remain in this application. Claims 1 and 2 have been amended. No claims have been cancelled or added.

Drawings

The Office Action requests new drawings. Applicants are submitting herewith formal drawings.

Rejections Under 35 U.S.C. § 103

The Office Action has rejected claims 1-4 under 35 U.S.C. § 103(a) as being unpatentable over Beausoliel et al., U.S. Patent No. 5,551,013 (hereinafter "Beausoliel") in view of Austin et al., U.S. Patent No. 4,885,684 (hereinafter "Austin"). Applicant respectfully traverses this rejection. Firstly, the Office Action incorrectly states that Beausoleil teaches compiling a user's design to include "blocking codes". All the section from Beausoleil quoted by the Office Action states is that the user's design is compiled into a series of control words (Col. 10, line 64 to Col. 11, line 2). Beausoleil, however, says nothing about the insertion of blocking codes, which by definition are not part of a user's design. Likewise, Beausoleil does not teach or suggest anything relating to decoding the blocking codes. Because Beausoleil does not teach or suggest that blocking codes should be compiled into a user's design, it only stands to reason that the non-existent blocking codes cannot be decoded. Austin does not supply any teachings to make up for Beausoleil's lack of teachings regarding blocking codes, as Austin teaches nothing of the sort. Indeed, Austin, which teaches a general purpose computer, would

not even be compiling a user's design into a series of instructions that could be executed by the emulator to mimic the design of a integrated circuit. Because of this, Austin would not teach or suggest anything relating to blocking codes that disable the main data memories and allows those memories to be updated via the maintenance bus.

Moreover, neither Beausoleil nor Austin teach or suggest how data is blocked and data is transferred as in claim 1. Claim 1 requires that the blocking code be decoded. Once the blocking code is decoded, claim 1 requires that "transfers between the plurality of module processors and said module main memory" be blocked and that data be transferred while the blocking condition exists. Neither Austin nor Beausoliel teach or suggest this. In particular, Austin neither teaches nor suggests decoding in response to decoding blocking code. The sections from Austin relied upon in the Office Action make no such teachings. In particular, the discussion at columns 6 and 7 in Austin only discuss management of the computer system disclosed therein. There is no discussion of disabling memory activities while they are updated. The same is true for the discussion at columns 12-13 in Austin. Col. 12, line 47 through Col. 13, line 7 relate to error correction and fault tolerance. This discussion says nothing about blocking codes that disable main data memories while they are updated. It bears noting that nothing in the present application suggests that the blocking codes are used.

It is also worth reiterating that neither Beausoliel nor Austin teach or suggest enabling transfers of external data to and from a module's main data memories without interrupting emulation in progress. Firstly, Beausoleil does not disclose any such feature. More importantly, Austin cannot supply such teachings since it is not even directed to emulation of user designs.

These same arguments apply to Claims 2-4, as they all are dependent on claim 1. Therefore, Applicant respectfully submits that claims 2-4 are allowable as well.

Based on the foregoing, Applicant respectfully submits that this application is in condition for allowance, which is respectfully requested.

Should the Examiner have any questions or comments on the application, the Examiner should feel free to contact the undersigned via telephone.

Respectfully submitted,

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Dated: October 24, 2003 By: _____

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